WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising:

a combination circuit, and

a scan diagnosis circuit capable of performing a scan test of said combination circuit;

wherein

said scan diagnosis circuit comprises:

a first scan chain having a plurality of scan flip-flops connected for operating in synchronization with a clock signal;

a second scan chain placed behind said first scan chain, and having a plurality of scan flip-flops connected for operating in synchronization with the clock signal;

a first clock buffer for supplying the clock signal in the direction opposite to the flow direction of scan test data that passes through said first scan chain;

a second clock buffer for supplying the clock signal in the direction opposite to the flow direction of scan test data that passes through said second scan chain; and

a return path for sending the scan test data output from a scan flip-flop placed at the closest position to said first clock buffer in said first scan chain to the

scan flip-flop placed at the furthermost position from said second clock buffer in said second scan chain.

2. A semiconductor integrated circuit according to claim 1, wherein

said return path is formed of a wiring finer than the feeder line of said clock signal.

3. A semiconductor integrated circuit according to claim 1, wherein

when the circuit has multilayered wirings and the resistance for unit length is different between layers, said return path is formed of a wiring having the resistance higher than the wirings forming the feeder line of said clock signal.

4. A semiconductor integrated circuit according to any one of claims 1 to 3, wherein

an area for inserting delay elements on the scan test data path in said return path is predefined to insert said delay elements in the area.

5. A semiconductor integrated circuit according to any one of claims 1 to 4, further comprising

a clock buffer for scan test, capable of delaying the

output signal of said first clock buffer; and

a selector, capable of supplying the output signal of said clock buffer for scan test instead of the output from said first clock buffer at the time of scan test by using said scan chain.

6. A semiconductor integrated circuit comprising:

a scan diagnosis circuit capable of performing a scan test of circuit, wherein

said scan diagnosis circuit includes a clock buffer, and a plurality of scan flip-flops dispersed on the area to which the clock signal is supplied from said clock buffer; and

said scan diagnosis circuit has a scan chain connection in the order of the scan flip-flop having the largest delay of the clock signal from said clock buffer to said scan flip-flop.

7. A semiconductor integrated circuit comprising:

a combination circuit, and

a scan diagnosis circuit capable of performing a scan test of said combination circuit;

said schematic circuit diagram comprising:

a plurality of first flip-flops having first clock signal line connected;

a plurality of second flip-flops having second clock signal line connected;

a first clock buffer connected to said first clock signal line; and

a second clock buffer connected to said second clock signal line;

wherein

said first clock buffer supplies a first clock signal to said first clock signal line;

said second clock buffer supplies a second clock signal to said second clock signal line;

said plurality of first flip-flops is formed on a first virtual line extending in a first direction, having data transferred from one end to the other end of said plurality of first flip-flops at the time of scan test;

said plurality of second flip-flops is formed on a second virtual line, which is in parallel to said first virtual line, having data from one end to the other end of said plurality of second flip-flops at the time of scan test;

data output from the other end of said plurality of first flip-flops is input to the one end of said plurality of second flip-flops;

said first clock buffer is configured such that the distance from said first clock buffer to the other end of said plurality of first flip-flops is shorter than the

distance from said first clock buffer to the one end of said plurality of first flip-flops; and

said second clock buffer is configured such that the distance from said second clock buffer to the other end of said plurality of second flip-flops is shorter than the distance from said second clock buffer to the one end of said plurality of second flip-flops.

8. A semiconductor integrated circuit according to claim 7, further comprising:

a third clock buffer for supplying the clock signal in common for said first clock buffer and said second clock buffer.

9. A semiconductor integrated circuit according to claim 7, wherein

the resistance of wiring for connecting the other end of said plurality of first flip-flops with the one end of said plurality of second flip-flops is larger than the resistance of said first clock signal wiring and of said second clock signal wiring.

10. A semiconductor integrated circuit according to claim 9, wherein

the wiring for connecting the other end of said

plurality of first flip-flops with the one end of said plurality of second flip-flops is finer than said first clock signal wiring and said second clock signal wiring.

11. A semiconductor integrated circuit according to claim 7, wherein

said combination circuit is provided between said plurality of first flip-flops and said plurality of second flip-flops.

12. A semiconductor integrated circuit according to claim 7, further comprising

a fourth clock buffer connected to said second clock buffer, and

a selector for selecting either one of the path for supplying said second clock signal directly from said second clock buffer to said plurality of second flip-flops or the path for supplying said second clock signal through said second and fourth clock buffers to said plurality of second flip-flops.